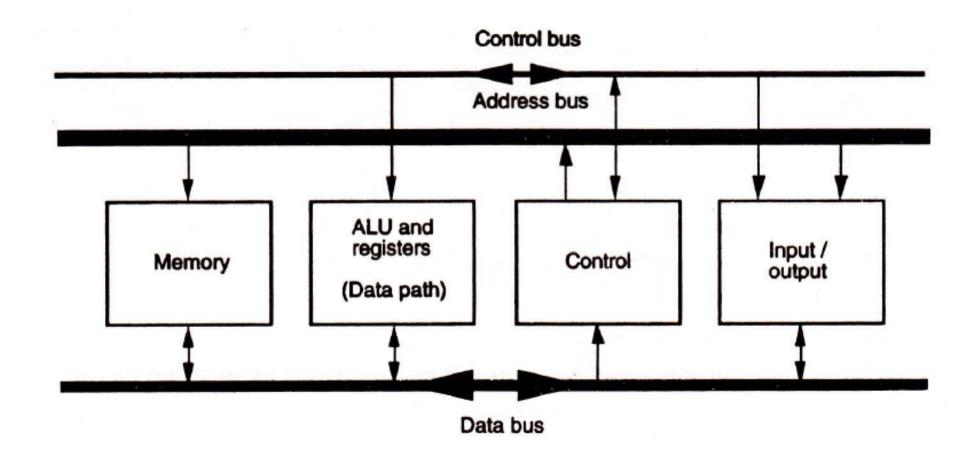
## Design Example

## 4-bft Arithmetic Processor

 The 4-bit microprocessor has been chosen as a design example because it is particularly suitable for illustrating the design and interconnection of common architectural blocks.



- Metal can cross polysilicon or diffusion without any significant effect
- Wherever polysilicon crosses diffusion a transistor will be formed.
   This includes the second polysilicon layer for processes that have two.
- Wherever lines touch on the same level an interconnection is formed.
- Simple contacts can be used to join diffusion or polysilicon to metal.
- To join diffusion and polysilicon we must use either a buried contact or a butting contact (in which case all three layers are joined together at the contact) or two contacts, diffusion to metal then metal to polysilicon.
- In some processes, a second metal layer is available. This can cross over any other layers and is conveniently employed for power rails.
- First and second metal layers may be joined using a via.
- Each layer has particular electrical properties which must be taken into account.
- For CMOS layouts, p- and n-diffusion wires must not directly join each other, nor may they cross either a p-well or an n-well boundary.

## Carry look ahead adder

 We have considered some other methods of improving adder throughput time and may now turn to algebra to seek a general solution to this problem. This is to be found in rearranging the expressions for the adder

$$C_k = A_k B_k + H_k . C_{k-1}$$

$$C_k = A_k . B_k + (A_k + B_k) . C_{k-1}$$

$$c_k = g_k + p_k . g_{k-1} + p_k . p_{k-1} g_{k-2} + \dots + p_k \dots p_1 . g_0 + p_k \dots p_0 . c_{in}$$

$$c_0 = g_0 + p_0.c_{in}$$

$$c_1 = g_1 + p_1.g_0 + p_1.p_0.c_{in}$$

$$c_2 = g_2 + p_2.g_1 + p_2.p_1.g_0 + p_2.p_1.p_0.c_{in}$$

$$c_3 = g_3 + p_3.g_2 + p_3.p_2.g_1 + p_3.p_2.p_1.g_0 + p_3.p_2.p_1.p_0.c_{in}$$

